. ATTACHMENT A: SEARCH HISTORY

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6222	latch and synchronous and communication and interface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L2	357	(latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L3	3119	(latch and synchronous and communication and interface ) and (memory with controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L4	1134	((latch and synchronous and communication and interface ) and (memory with controller)) and (delay same circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L5	130	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and ((latch and synchronous and communication and interface ) and (memory with controller)) and (delay same circuit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L6	233	latch and synchronous and communication and interface and SDRAM and DDR	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L7	2	("6442102").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L8	25	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and SDRAM and DDR	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L9	26	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45

1323   data same latch) and synchronous and communication and interface and (data same strobe same signal)   US-PGPUB;							
and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable and (synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and Synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and SPRAM  L13 33 (((data same latch) and Synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and "365"\\$7.  L14 7027 ((memory same controller) and latch and synchronous and communication and synchronous) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gotheronous same data same strobe same signal)) and (gotheronous same data same strobe same signal) and multiplex\$  L18 5 ((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and multiplex\$  L18 5 ((latch and synchronous and communication and interface) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and disable and (data same strobe same signal) and disable and (data same strobe same signal) and communication and interface and strobe same signal) and disable and (data same strobe same signal) and communication and interface and strobe same signal) and communication and interface a	L10	1323	and communication and interface	USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
Synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and SDRAM  L13 33 ((((data same latch) and synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and "365"/\$7. ccls.  L14 7027 (memory same controller) and latch and synchronous and (gate with circuit) and disable and (data same strobe same signal)) and (SDRAM or DDR)  L15 85 ((((memory same controller) and latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal)) and (SDRAM or DDR)  L16 379 (((memory same controller) and latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal))  L17 20 (((latch and synchronous and communication and interface) and (data same strobe same signal)) and (synchronous same data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (data same strobe same signal)) and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal) and communication and interface ) and (data same strobe same signal)) and (synchronous same data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal) and communication and interface ) and (data same strobe same signal) and counter and (burst with length)  L19 2 "6442102".URPN.  USPAT PO; JPO; DCRWENT; IBM_TDB  US-PGPUB; USPAT; EPO; JPO; DCRWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DCRWENT; IBM_TDB	L11	346	and communication and interface and (data same strobe same signal)) and (gate with circuit) and	USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and "365"/\$7. ccls.  L14 7027 (memory same controller) and latch and synchronous ((((memory same controller) and latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal)) and (SDRAM or DDR)  L16 379 (((memory same controller) and latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal)) and (synchronous and communication and interface) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and counter and (burst with length)  L19 2 "6442102".URPN. USPAT OR OFF 2005/05/02 04:45	L12	41	synchronous and communication and interface and (data same strobe same signal)) and (gate with	USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
and synchronous  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB  US-PGPUB; OR OFF 2005/05/02 04:45  USPAT; EPO; JPO; DERWENT; IBM_TDB	L13	33	synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and "365"/\$7.	USPAT; EPO; JPO; DERWENT;	OR	OFF	
latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal)) and (SDRAM or DDR)  L16 379 ((memory same controller) and latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal)  L17 20 ((latch and synchronous and communication and interface) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal)) and (synchronous and communication and interface) and (gate with circuit) and multiplex\$  L18 5 ((latch and synchronous and communication and interface) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal)) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal)) and (synchronous same data same strobe same signal) and communication and interface) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and counter and (burst with length)  L19 2 "6442102".URPN. USPAT OR OFF 2005/05/02 04:45	L14	7027		USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
L17  20 ((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal))  L17  20 ((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and multiplex\$  L18  5 ((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal) and multiplex\$  US-PGPUB;	L15	85	latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal)) and	USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and multiplex\$  L18  5 ((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and counter and (burst with length)  L19  2 "6442102".URPN.  USPAT; EPO; JPO; DERWENT; EPO; JPO; DERWENT; IBM_TDB  USPAT; EPO; JPO; DERWENT; IBM_TDB	L16	379	latch and synchronous) and (gate with circuit) and disable and (data	USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and counter and (burst with length)  L19  2 "6442102".URPN.  USPAT; -EPO; JPO; DERWENT; IBM_TDB  USPAT OR OFF 2005/05/02 04:45	L17	20	communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same	USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
	L18	5	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and counter	USPAT; •EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
L20 2 "6442102".URPN. USPAT OR OFF 2005/05/02 04:45	L19	2	"6442102".URPN.	USPAT	OR	OFF	2005/05/02 04:45
	L20	2	"6442102".URPN.	USPAT	OR	OFF	2005/05/02 04:45

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L21	2	"6442102".URPN.	USPAT	OR	OFF	2005/05/02 04:45
L22	2	("6147927"   "6316980").PN.	USPAT	OR	OFF	2005/05/02 04:45
L23	6222	latch and synchronous and communication and interface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L24	357	(latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L25	3119	(latch and synchronous and communication and interface ) and (memory with controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L26	1134	((latch and synchronous and communication and interface ) and (memory with controller)) and (delay same circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	OFF	2005/05/02 04:45
	. :		IBM_TDB			
L27	1323	(data same latch) and synchronous and communication and interface and (data same strobe same signal)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L28	346	((data same latch) and synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L29	7027	(memory same controller) and latch and synchronous	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L30	20	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and multiplex\$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L31	2	"6442102".URPN.	USPAT	OR	OFF	2005/05/02 04:45
L32	, 2	"6442102".URPN.	USPAT	OR	OFF	2005/05/02 04:45
L33	2	"6442102".URPN.	USPAT	OR	OFF	2005/05/02 04:45

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L34	2	("6442102").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L35	25	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and SDRAM and DDR	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L36	26	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L37	41	(((data same latch) and synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and SDRAM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L38	33	(((data same latch) and synchronous and communication and interface and (data same strobe same signal)) and (gate with circuit) and disable) and "365"/\$7. ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L39	85	(((memory same controller) and latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal)) and (SDRAM or DDR)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L40	5	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and (synchronous same data same strobe same signal) and counter and (burst with length)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L41	2	("6147927"   "6316980").PN.	USPAT	OR	OFF	2005/05/02 04:45
L42	130	((latch and synchronous and communication and interface ) and (gate with circuit) and disable and (data same strobe same signal)) and ((latch and synchronous and communication and interface ) and (memory with controller)) and (delay same circuit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45

1.42	222		LIC DCDLID.	OD	٥٢٢	2005/05/02 04:45
L43	233	latch and synchronous and communication and interface and SDRAM and DDR	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 04:45
L44	379	((memory same controller) and latch and synchronous) and (gate with circuit) and disable and (data same strobe same signal)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 07:22
L45	379	44 and disabl\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 07:23
L46	377	45 and receiv\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 07:23
L47	377	46 and (data same strobe)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 07:24
L48	87	47 and 365\$7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/02 07:24